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Resume

Name:	Michael Timothy Moore
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Occupation:
I am a patent agent with Cypress Semiconductor Corp, working in the legal group. I am a qualified US patent agent, registration number 53346. My role includes the preparation and prosecution of US patents, research of third-party products and patents to determine possible infringement, and preparation and review of IP licensing contracts. I have worked in this role for over a year.

Prior to this I was a Senior Applications Engineer with Cypress in the Data Communications (Datacom) Division for over three years. My work was in the area of data and voice communications over SONET and SDH, and also in the development and licensing of IP products for Cypress.

Legal Status:
I am a US permanent resident; I hold a 'green card' visa.

Education:
I hold an MBA (specializing in Finance) from Santa Clara University I graduated in June 2003.

I hold a Bachelor's degree in Electronic Engineering from the University of Limerick, Ireland. This was a four-year course, from September 1994 to June 1998.

Accomplishments
I hold three US patents (6,481,001, 6,452,417, and 6,538,468) and I have filed another seven US patents for inventions in the area of data communications and programmable logic architecture and software.

I have authored over twenty technical and marketing-related articles published in influential industry journals in the US, Europe and Asia, including EDN and EETimes.

I speak fluent business level French and I hold a fluency qualification from the Paris Chamber of Commerce and Industry (C.C.I.P.). I also speak fluent Gaelic, and conversational German. English is my native language.

Interests:
I enjoy windsurfing, swimming and snowboarding, along with most outdoors and water sports. I am a past member my University windsurfing team. Musically, I am an avid fan of Irish traditional music and jazz. I love cooking and particularly enjoy great Italian food.

Work experience:
Jan 2001 to Jan 2002:
From January 2001 to January 2001 I worked the Wide Area Networking (WAN) group in the Datacom Division of Cypress. I held the title of Senior Applications Engineer, responsible for Cypress' POSIC (Packet over SONET Integrated Circuit) SONET/SDH Framer product, where I developed expertise in a wide array of networking concepts and protocols. My role included representing my employer at important industry forums to develop the next generation telecommunications standards for data and voice networks.

June 1999 to Jan 2001:
Overall: My work from July 1999 to January of 2001 was with the Programmable Logic Group in the Datacom Division, as an Applications Engineer. I was the Project Leader for two projects to develop a family of intellectual property products (cores) for Cypress programmable logic devices. My role involved both the management and technical aspects of this project, supervising a student engineer, and directing the work of other engineers and 3rd party contractors.

Training: My role has also involved creation and presentation of training material for both internal and external customers. I have presented a several papers on efficient HDL coding and floorplanning at the Cypress technical conferences, and I have traveled internationally to present training courses to strategic customers.
Hiring: I organized and executed a two-week hiring trip to Ireland during November 2000. From this trip 13 offers were made, and four Datacom employees were hired.

August 1998 to June 1999:
During this period with Cypress I was responsible for developing an innovative design characterization platform for the newest generation of Cypress programmable logic products. I developed an efficient method for quickly and easily creating all the test software required to characterize the 37K family of devices. My technique resulted in much faster (days instead of weeks) preparation and modification of test software. With my developments I obtained characterization results within hours of receiving first silicon, instead of days or weeks which had been previously required. This project was very successful and gave Cypress a significant competitive advantage.

Work experience while in University, 1994 to 1998:
While I attended the University of Limerick, Ireland I worked both part time (during school semesters) and full-time (during summers) with the Design Evaluation Group in Analog Devices, Inc. in Limerick, Ireland.

Exhibit A

Electronics Engineers' Handbook

DONALD G. FINK *Editor*

Director Emeritus, Institute of Electrical and Electronics Engineers; Fellow, IEEE; Member of the National Academy of Engineering; Eminent Member, Eta Kappa Nu; Registered Professional Engineer; formerly Executive Director and General Manager, IEEE; Editor in Chief, Electronics; *Vice President—Research, Philco Corporation; President, Institute of Radio Engineers; Editor,* Proceedings of the IRE; *Fellow of the Institution of Electrical Engineers (London)*

DONALD CHRISTIANSEN *Editor*

Staff Director, Institute of Electrical and Electronics Engineers; Editor, IEEE Spectrum; *Fellow, IEEE; Member, IEEE Publications Board; Eminent Member, Eta Kappa Nu; Member, New York Academy of Sciences; Member, Royal Institution (London); Fellow, World Academy of Art and Science; Registered Professional Engineer; formerly Editor in Chief,* Electronics; *Engineering Group Leader, CBS Electronics*

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trajectory through the silicon the α particle generates roughly 1.2 million electron-hole pairs. Some percentage of the electrons generated will find their way to the surface and be collected by memory-cell nodes. If the number collected by any one node is large, the voltage on the node may be reduced sufficiently to cause a misread or soft failure. One source of the α particles is the IC packaging material, and efforts are being made to reduce the α radiation to a minimum. Another possible solution is to coat the surface of the IC with a material that will stop the α particle from getting to the silicon surface.

Figure 8-159 shows the organization diagram for a dynamic MOS RAM. Reading and writing occur for all cells in one row simultaneously. Since only 1 bit at a time is available for writing, an internal read operation is used to transfer the data to the refresh amplifier before writing. In this manner, the refresh amplifier contains data corresponding to the contents of the row into which writing takes place.[101]

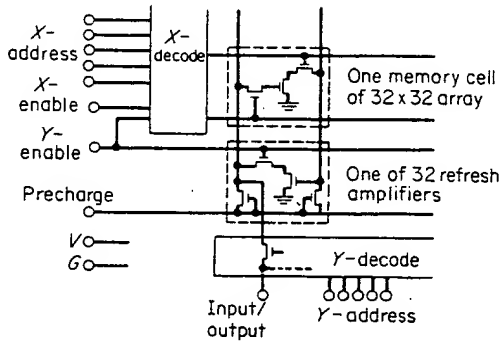

Fig. 8-159. Organization diagram of a dynamic MOS random-access memory system.

97. Shift Registers. A shift register is an arrangement of an arbitrary number of storage cells in a row and is used primarily for temporary storage of digital information. Some common applications of shift registers are in serial-data entry and serial-data output, as well as in serial-to-parallel converters. The serial-in–serial-out shift register can perform similarly to a high-speed drum memory; however, unlike the mechanical drum memory, it can be stopped instantaneously. Serial-to-parallel converters are often used in accumulators, where the data are entered in serial fashion, e.g., from a keyboard, and then acted upon in parallel, as by an adder.

The shift registers can be designed for either static or dynamic operation. Static shift registers make use of the basic flip-flop circuits of Figs. 8-146 and 8-147 for data-storage purposes. Dynamic shift registers operate in the same manner as the dynamic RAM circuits, where each bit of information is constantly refreshed and recycled. Figure 8-160 shows the circuit diagram of a section of a dynamic MOS shift-register circuit. The circuit operates with two-phase clock pulses, $V_{\phi 1}$ and $V_{\phi 2}$. After each clock pulse, one bit of information is inverted and transferred half a cell to the right; thus, after two clock pulses, the contents of each cell are shifted over to the next one.

98. Array Circuit Types. LSI logic arrays fall into two basic categories, *field-programmable* and *mask-programmable*,[109,110] each with important advantages and disadvantages. All field-programmable types have a fixed number of OR gates, AND gates, and sometimes flip-flops per circuit. Programming is handled through *fusible links* similar to those of a PROM. Advantages are that several custom logic functions can be developed from one IC part number by blowing the fuse links. Changes are easily incorporated by programming a new fuse pattern. Programming commonly requires special equipment, although some of the smaller array circuits use standard PROM programming hardware. Disadvantages of the fusible-link approach relate to the fixed pattern of inputs, outputs, and logic functions on chips. For example, an LSI circuit incorporating a 10-bit shift register cannot be built if the field-programmable circuit is limited to eight flip-flops. Similarly an LSI part requiring multiphase clocking cannot be built on an array which connects all flip-flops to a common clock line.

Mask-programmable arrays, commonly known as *gate arrays,* and *macrocell arrays* and sometimes called *master slices,* offer greater logic flexibility. Gate arrays have a large number of gates on chips which can be connected to build any logic function, subject only to package pins and the number of gates. By interconnecti elements can be placed in any combi

The *macrocell array* carries the co complexity blocks, called macrocells library of macrocell functions and ne

Disadvantages of mask-programma option requires a custom metal patte having only custom metal is much s full semiconductor mask set, it is n location.

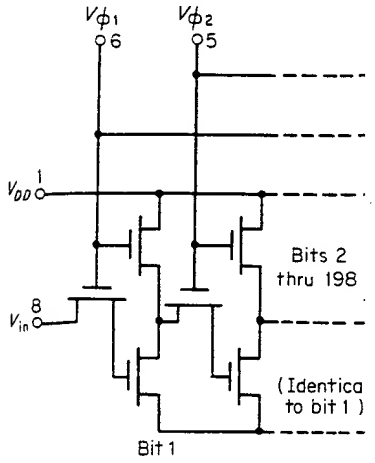

Fig. 8-160. Circuit diagra

Arrays approaching 1,200 gates hav generally better than with the mask p with ECL arrays, is superior to other

The main purpose of logic arrays is LSI circuit. One way of comparing th circuit board and see how each replac

The *fusible-link arrays* equate to a c sometimes flip-flops. The board is full the gates implement various logic equ

The *gate array* is the same circuit b gate packages. The designer than adds function.

The analogy can be extended to ma IC sockets and a data book full of log data book (macrocell library), puts th routing channels.

A typical macrocell array has 85 lo positions on the chips.

Array Terminology. The followi

Gate array: An IC containing a nur dedicated metal patterns to form a cu and 1,200 gates and may use CMOS,

Macrocell: An array subsection pe Macrocells normally relate to MSI co adders, etc., and make design easier t array or the basic building block in a

the number of gates. By interconnecting gates as flip-flops, adders, multiplexers, etc., these circuit elements can be placed in any combination anywhere on a chip.

The *macrocell array* carries the concept one step further by subdividing the array into MSI-complexity blocks, called macrocells, rather than individual gates. The designer works with a library of macrocell functions and need not implement everything from simple gates.

Disadvantages of mask-programmable arrays center around mask programming. Every circuit option requires a custom metal pattern on top of a standard semiconductor diffusion set. While having only custom metal is much simpler than a custom circuit designed from scratch with a full semiconductor mask set, it is more complex than programming with fuses at the user's location.

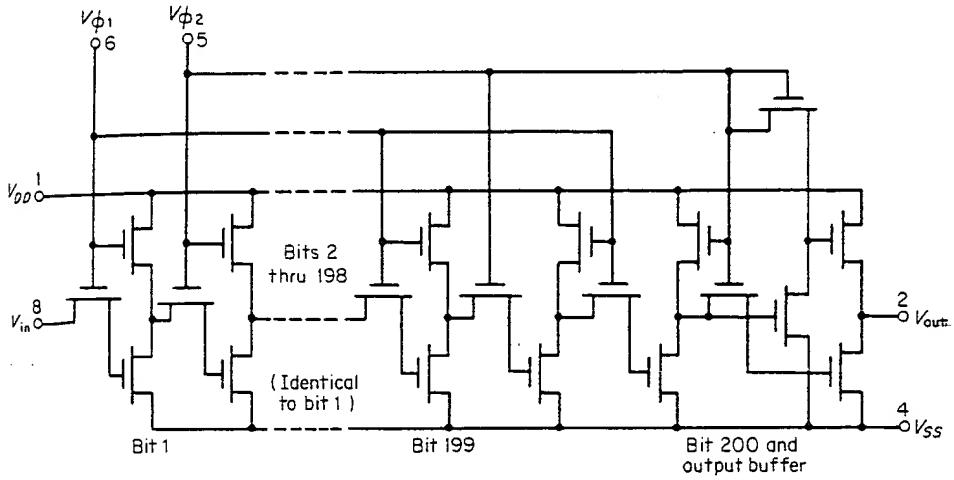

Fig. 8-160. Circuit diagram of one section of a 200-bit dynamic shift register.

Arrays approaching 1,200 gates have more logic power per package, speed-power products are generally better than with the mask programmable circuits, and circuit performance, especially with ECL arrays, is superior to other forms of digital logic.

The main purpose of logic arrays is to replace several IC packages on a circuit board with one LSI circuit. One way of comparing the array types is to visualize them as a miniature printed-circuit board and see how each replaces logic.

The *fusible-link arrays* equate to a circuit board with a combination of OR gates, AND gates, and sometimes flip-flops. The board is fully wired. The designer then cuts metal (fusible links) so that the gates implement various logic equations.

The *gate array* is the same circuit board populated with a large number of two- or three-input gate packages. The designer than adds metal, interconnecting the gates to implement the desired function.

The analogy can be extended to macrocell arrays by visualizing a circuit board full of empty IC sockets and a data book full of logic functions. The designer selects logic functions from the data book (macrocell library), puts them in the IC sockets, and interconnects the ICs through routing channels.

A typical macrocell array has 85 logic functions in a macrocell library and a total of 106 cell positions on the chips.

Array Terminology. The following definitions will be helpful:

Gate array: An IC containing a number of uncommitted gates which are interconnected with dedicated metal patterns to form a custom-circuit logic function. Gate arrays vary between 100 and 1,200 gates and may use CMOS, I^2L, TTL, or ECL circuit technologies.

Macrocell: An array subsection performing a higher-level logic function than a basic gate. Macrocells normally relate to MSI complexity circuits such as flip-flops, decoders, multiplexers, adders, etc., and make design easier than using gates. Macrocells can be several gates in a gate array or the basic building block in a more advanced macrocell array.